PATENT
Attorney Docket No. INT04-001US(P2083US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Peter Onody

Art Unit: 2816

Application No. 10/817,499

Examiner: Le, Dinh Thanh

Filed: 04/02/2004

For: TUNABLE SALLEN-KEY FILTER STAGE AND FILTER ASSEMBLY

APPELLANT'S APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In support of the appeal from the final rejection dated January 30, 2006, Appellant now submits his Brief.

This is an appeal from the Final Rejection of Examiner Le mailed January 30, 2006 rejecting all of the pending claims of the case. This brief is accompanied by the requisite fee set forth in 37 C.F.R. § 1.17(c). The Notice of Appeal was filed on April 25, 2006.

Real Party In Interest

The patent application that is the subject of this appeal is assigned to INTEGRATION ASSOCIATES INC.

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Related Appeals and Interferences

There are no appeals or interferences that are related to this appeal.

Status of Claims

Claims 21, 22 and 25-50 are pending in the application. Claims 21, 22 and 25-50 stand rejected. Claims 21, 22 and 25-50 and are the subject of this appeal.

Claims 1-49 were originally filed. Claims 1-20 were withdrawn per an election made in response to a restriction requirement. Claims 23 and 24 were cancelled by amendment. Claim 50 was added by amendment. Claims 21 and 41 are in independent form.

Status of Amendments

All amendments in the application have been entered.

Summary of Invention

In the specification as originally filed, Figure 1 shows a filter assembly where the tuning of the filter stages 10_1-10_n is done with the help of the digitally controlled oscillator (DCO) circuit 40, via the SAR circuit 50, where the latter directly controls the bus 60. The DCO circuit 40 includes an RC oscillator, and the output frequency of the DCO 40 is a function of the resistor value in the RC oscillator. The resistor of the RC oscillator in the DCO 40 is variable and the variable resistors of the filter stages is substantially identical to the structure of the variable resistor of the RC oscillator. (¶14, ¶49, ¶50).

The SAR circuit 50 performs the functions of a resistor setting circuit, in the sense that it sets directly, by way of the bus 60, the resistance values of the variable resistors in both the DCO 40 and in the filter stages. The SAR circuit 50 contains a successive approximation register, which changes its output until the two input frequencies – one from the DCO circuit 40, the other from the reference oscillator 30 – are equal. As shown in Figure 1, the output of the SAR 50 directly controls the bus 60, i.e. it is the SAR circuit that sets the values of the resistors in the filter stages, and simultaneously in the DCO itself, because the bus 60 switches simultaneously all the resistors banks that are controlled by the bus 60, i.e. the controlled resistor banks will assume equal or at least more or less linearly proportional resistance values. In other words, the output of the RC oscillator controls the value of the variable resistors in the filter stages, but this controlling output of the RC oscillator also controls the value of the variable resistor of the RC oscillator itself. (¶60)

In one embodiment, the present invention is directed toward a filter circuit assembly having at least one filter stage (see 10_n in Figure 1, Figure 3, Figure 4, ¶ 22), where the filter stage includes at least one variable resistor (see R11, R21, R12 and R22 of Figures 3 and 4, ¶¶ 27-28, 34, 38, 41, 42 and 46). The assembly also includes a resistor/capacitor (RC) oscillator (40, see Figures 1 and 5) having an output, where the RC oscillator includes at least one variable resistor (R_{DCO}, Figure 5, ¶50). A successive approximation register (50) is

coupled to the output of the RC oscillator (40) that generates a control value corresponding to the output of the RC oscillator. The control value of the successive approximation register (50) controls the resistance of the variable resistor of the filter stage (R11, R21, R12 and R22) and the resistance of the variable resistor (R_{DCO}) of the RC oscillator (¶60). Further, the variable resistor of the filter stage and the variable resistor of the RC oscillator have a substantially identical structure (¶¶50-51). Each variable resistor structure is closely coupled to a power supply terminal (V_{dd}) of the filter circuit assembly and includes a plurality of resistors coupled in series with one another (Figure 7, BR1, BR2, BR3, BRq, ¶¶46-47) and a plurality of transistors (SR1, SR2, SR3, SRq), each transistor coupled in parallel with a corresponding one of the plurality of resistors, where a gate of each transistor is coupled to a corresponding bit of the successive approximation register (¶¶50-51).

In another embodiment, the present invention is directed toward a method for adjusting the frequency or compensating process parameters of a Sallen-Key type filter (¶49, ¶60) having at least one filter stage (see 10_n in Figure 1, Figure 3, Figure 4, ¶ 22) with variable resistors (see R11, R21, R12 and R22 of Figures 3 and 4, ¶¶ 27-28, 34, 38, 41, 42 and 46). The method includes providing an RC oscillator (40, see Figures 1 and 5) having an output. The RC oscillator has at least one variable resistor (R_{DCO}, Figure 5, ¶50), where the variable resistor of the filter stage and the variable resistor of the RC oscillator have a substantially identical structure (¶¶50-51). Each variable resistor structure is closely coupled to a power supply terminal (V_{dd}) of the filter stage and the RC oscillator (¶¶46-47). The method then calls for controlling the resistance of the variable resistor of a filter stage with the output of the RC oscillator and controlling the resistance of the variable resistor of the RC oscillator with the output of the RC oscillator (¶49, ¶60).

Issues

Claims 21, 22, 25-33, 41-45 and 48 stand rejected under 35 U.S.C. §102(e) as being anticipated by Pham (U.S. Patent No. 6,803,813). Claims 34-40, 46-47 and 49-50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pham in view of Figure 2 of Appellant's admitted prior art.

Grouping of Claims

Claims 21, 22, 25, 27-33 and 34-35, 38-50 stand or fall together. Claim 26 stands or falls independently. Claims 36 and 37 stand or fall together.

Argument

Appellant traverses the rejections. The primary reference relied upon by the Examiner, Pham, does not teach or suggest an RC oscillator as recited in the claims. Pham merely discloses a tunable impedance circuit. Therefore, the reference relied upon does not anticipate claims 21, 22, 25-33, 41-45 and 48. Further the combination cited by the Examiner (Pham and Figure 2 of the Appellant's specification) also fails to teach or suggest the claimed oscillator as set forth in claims 34-40, 46-47 and 49-50.

The primary reference relied upon fails to teach the claimed oscillator, as asserted by the Examiner.

The Examiner asserts that Pham discloses a resistor/capacitor (RC) oscillator (102). However, the Pham reference clearly contradicts the Examiner. Pham states that the "**tunable impedance circuit** 102 is an RC circuit" that includes "a tunable resistive circuit 102r ... and a substantially fixed capacitive circuit 102c." Col. 4, line 55 et seq., *emphasis added.* "The terminal voltage V_C across the capacitive circuitry 102c is reset by a shunt switch 102s every half cycle of an **external clock signal** CLK1 having a clock signal frequency f_{CLK1}." Col. 5, line 13 et seq., *emphasis added.* And, finally, "the voltage VC across the capacitive crciutry 102c is **a ramp signal** which will be reset during the time that the clock signal CLK1 is asserted." Col. 5, line 23 et seq., *emphasis added.* Pham appears to describe a circuit for generating a ramp signal in response to an externally supplied clock signal – not an oscillator, as claimed by the Examiner.

It appears that the claimed oscillator is absent from the reference relied upon by the Examiner. Therefore, the reference does not teach each and every element of the invention as set forth in claims 21-22, 25-33, 41-45 and 48 and does not anticipate these claims. Also, the Examiner relies on Pham for the teaching of an oscillator in the combination asserted by the Examiner in rejecting claims 34-40, 46-47 and 49-50 for unpatentability. Because there is no teaching or suggestion for an oscillator in the proposed combination, no prima facie case for obviousness has been established for claims 34-40, 46-47 and 49-50.

Claim 26

In addition, with regard to claim 26, which stands rejected under 35 U.S.C. §102(e), the Examiner asserts that Pham shows that the substantially constant current (IR) is mirrored

for alternatingly charging and discharging a capacitor 102c of the RC oscillator. However, not only does Pham contain no teaching for an oscillator, but Pham contradicts the Examiner's assertion regarding the charging and discharging of the capacitor. Specifically, Pham teaches that "[t]he terminal voltage V_C across the capacitive circuitry 102c is reset by a shunt switch 102s every half cycle of an external clock signal CLK1 having a clock signal frequency f_{CLK1}." Col. 5, line 13 et seq. Unlike the invention, as claimed in claim 26, the voltage across capacitive circuitry 102c is discharged by the external clock signal closing a switch rather than a mirrored current. The absence of a teaching in the reference relied upon for the limitation of claim 26 wherein "the substantially constant current is mirrored by current mirrors for alternatingly charging and discharging a capacitor of the RC oscillator" represents an additional basis for the patentability of claim 26 over the Pham reference relied upon by the Examiner.

Claims 36-37

Further, with regard to claims 36-37, which stand rejected under 35 U.S.C. §103(a), the Examiner asserts that the capacitors 116c of Pham are tunable capacitors. However, there appears to be no teaching in Pham for tunable or variable capacitors. Pham states that 102c is a substantially fixed capacitive circuit. Col. 4, lines 55-62. There appears to be no teaching in Pham for tunable capacitors – the symbol for 116c in Figure 3 does not include a diagonal arrow to indicate variability, as do variable resistor circuits 102r and 116r. The absence of a teaching in the reference relied upon for the additional limitation of claims 36 and 37 "wherein the at least one filter stage comprises a variable capacitor" represents an additional basis for the patentability of claims 36 and 37 over the Pham reference relied upon by the Examiner.

Conclusion

The reference relied upon by the Examiner fails to teach the elements of the claimed invention. Consequently, the Pham reference does not anticipate the invention of claims 21-22, 25-33, 41-45 and 48. Further, the combination of references asserted by the Examiner also fails to teach or suggest all of the elements of the invention of claims 34-40, 46-47 and 49-50 and no prima facie case for obviousness has been established by the Examiner with respect to these claims. For the foregoing reasons, Appellant submits that the Examiner's rejection of the pending claims is erroneous. Accordingly, Appellant respectfully requests that the board reverse the Examiner's rejection of claims 21, 22 and 25-50.

Respectfully submitted,

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Date: June 23, 2006

CLAIMS APPENDIX

Claims 1-20 (Withdrawn)

21. (Previously presented) A filter circuit assembly comprising:

at least one filter stage, said filter stage comprising at least one variable resistor,

a resistor/capacitor (RC) oscillator having an output, said RC oscillator further comprising at least one variable resistor;

a successive approximation register coupled to the output of the RC oscillator and generating a control value corresponding to the output of the RC oscillator, where the control value of the successive approximation register controls the resistance of the variable resistor of the filter stage and the resistance of the variable resistor of the RC oscillator;

wherein the variable resistor of the filter stage and the variable resistor of the RC oscillator have a substantially identical structure, where each variable resistor structure is closely coupled to a power supply terminal of the filter circuit assembly, and the variable resistor structure comprises a plurality of resistors coupled in series with one another and a plurality of transistors, each transistor coupled in parallel with a corresponding one of the plurality of resistors, where a gate of each transistor is coupled to a corresponding bit of the successive approximation register.

22. (Original) The assembly of claim 21, wherein the RC oscillator further comprises an RC digitally controlled oscillator (DCO).

23. (Canceled) The assembly of claim 21, wherein the variable resistors comprise multiple switchable resistors

24. (Canceled) The assembly of claim 21, wherein the substantially identical structure of the variable resistors comprises the connection layout and the value of the respective resistors within the variable resistors.

25. (Previously presented) The assembly of claim 21, wherein voltage across the variable resistor of the RC oscillator is substantially constant, so that a substantially constant current flows through the variable resistor.

26. (Previously presented) The assembly of claim 25, wherein the substantially constant current is mirrored by current mirrors for alternatingly charging and discharging a capacitor of the RC oscillator.

27. (Previously presented) The assembly of claim 21, further comprising

a reference oscillator having an output,

a resistor setting circuit having a first input for receiving the controlling output of the RC oscillator and a second input for receiving said output of the reference oscillator,

wherein the controlling output of the resistor setting circuit controls the resistance of the variable resistors of the filter stage and the RC oscillator.

28. (Original) The assembly of claim 27, wherein the controlling output of the RC oscillator delivers a frequency of the RC oscillator.

29. (Original) The assembly of claim 28, wherein the frequency of the RC oscillator is a function of the variable resistor of the RC oscillator.

30. (Original) The assembly of claim 21, wherein the frequency of the RC oscillator is proportional to the frequency of the filter stage.

31. (Original) The assembly of claim 27, wherein the resistor setting circuit is a successive approximation register (SAR) circuit.

32. (Original) The assembly of claim 27, wherein the resistor setting circuit adjusts its controlling output as a function of the frequency of the RC oscillator and the frequency of the reference oscillator.

33. (Previously presented) The assembly of claim 32, wherein the resistor setting circuit adjusts values of the variable resistors until the frequency of the RC oscillator and the frequency of the reference oscillator assumes a predetermined proportion.

34. (Original) The assembly of claim 21, comprising multiple filter stages.

35. (Previously presented) The assembly of claim 34, in which the at least one filter stage comprises a filter circuit, the filter circuit comprising

an amplifier part, the amplifier part having a positive input, a negative input, a positive output, a negative output,

first and second resistors connected in series with the positive input of the amplifier part, having a first node between said first and second resistors, the second resistor being connected between the first resistor and the positive input of the amplifier part,

third and fourth resistors connected in series with the negative input of the amplifier part, having a second node between said third and fourth resistors, the fourth resistor being connected between the third resistor and the negative input of the amplifier part,

at least one capacitor connected between the positive and negative inputs of the amplifier part,

first and second feedback capacitor connected between the first and second nodes and the positive and negative outputs of the amplifier part,

an input buffer part, the input buffer part having a positive input, a negative input, a positive output, a negative output,

the input buffer part further comprising a first buffer output resistor associated to the positive output of the input buffer part, a second buffer output resistor associated to the negative output of the input buffer part,

wherein the first and third resistors comprise the first and second buffer output resistors, respectively.

36. (Previously presented) The assembly of claim 34, wherein the at least one filter stage comprises a variable capacitor.

37. (Original) The assembly of claim 35, wherein the variable capacitor comprises multiple switchable capacitors

38. (Original) The assembly of claim 37, wherein the assembly is implemented on a chip.

39. (Original) The circuit assembly of claim 35, wherein said first and second output buffer resistors are connected in series with said first and third resistors, respectively.

40. (Original) The circuit assembly of claim 21, wherein a required supply voltage of the assembly is not higher than 1.5 V.

41. (Previously presented) A method for adjusting the frequency or compensating process parameters of a Sallen-Key type filter having at least one filter stage with variable resistors, the method including the steps of

providing an RC oscillator having an output, said RC oscillator further comprising at least one variable resistor, wherein the variable resistor of the filter stage and the variable resistor of the RC oscillator have a substantially identical structure, where each variable resistor structure is closely coupled to a power supply terminal of the filter stage and the RC oscillator,

controlling the resistance of the variable resistor of a filter stage with the output of the RC oscillator,

controlling the resistance of the variable resistor of the RC oscillator with the output of the RC oscillator.

42. (Previously presented) The method of claim 41, further comprising the ~~step~~ steps of

providing a reference oscillator having an output,

providing a resistor setting circuit having a first input for receiving the controlling output of the RC oscillator and a second input for receiving said output of the reference oscillator, and a controlling output,

the method further comprising the step of controlling the resistances of the variable resistors of the filter stage and the RC oscillator with the controlling output of the resistor setting circuit.

43. (Original) The method of claim 42, further comprising the step of delivering the frequency of the RC oscillator to the controlling output of the RC oscillator.

44. (Original) The method of claim 42, further comprising the step of adjusting the controlling output of the resistor setting circuit as a function of at least one of the following:
a, the frequency of the RC oscillator
b, the frequency of the reference oscillator.

45. (Previously presented) The method of claim 44, further comprising the step of adjusting the resistances of the variable resistors until the frequency of the RC oscillator and the frequency of the reference oscillator assumes a predetermined proportion.

46. (Previously presented) The method of claim 41, further comprising the step of employing a filter circuit with multiple filter stages, wherein a filter stages comprises

an amplifier part, the amplifier part having a positive input, a negative input, a positive output, a negative output,

first and second resistors connected in series with the positive input of the amplifier part, having a first node between said first and second resistors, the second resistor being connected between the first resistor and the positive input of the amplifier part,

third and fourth resistors connected in series with the negative input of the amplifier part, having a second node between said third and fourth resistors, the fourth resistor being connected between the third resistor and the negative input of the amplifier part,

at least one capacitor connected between the positive and negative inputs of the amplifier part,

first and second feedback capacitor connected between the first and second nodes and the positive and negative outputs of the amplifier part, respectively,

an input buffer part, the input buffer part having a positive input, a negative input, a positive output, a negative output,

the input buffer part further comprising a first buffer output resistor associated to the positive output of the input buffer part, a second buffer output resistor associated to the negative output of the input buffer part,

the method further including the step of including the resistances of said first and second buffer output resistors in the resistances of said first and third resistors, respectively.

47. (Original) The method of claim 46, further including the step of connecting said first and second buffer output resistors in series with said first and third resistors.

48. (Original) The method of claim 41, further including the step of providing a substantially constant voltage across the variable resistor in the RC oscillator, and thereby generating a substantially constant current flowing through the variable resistor.

49. (Original) The method of claim 48, further including the step of mirroring said substantially constant current for alternatingly charging and discharging a capacitor in the RC oscillator.

50. (Previously presented) The method of claim 41, wherein the substantially identical structure of the variable resistors comprises a plurality of resistors coupled in series with one another and a plurality of transistors, each transistor coupled in parallel with a corresponding one of the plurality of resistors, where a gate of each transistor is controlled by the output of the RC oscillator

AF/IDW

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Peter Onody

Art Unit: 2816

Application No. 10/817,499

Examiner: Le, Dinh Thanh

Filed: 04/02/2004

For: TUNABLE SALLEN-KEY FILTER STAGE AND FILTER ASSEMBLY

TRANSMITTAL OF
APPELLANT'S APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In accordance with 37 CFR 1.192, appellant hereby submits Appellant's Brief on Appeal in triplicate.

The items checked below are appropriate:

1. Status of Appellant

This application is on behalf of ☐ other than a small entity or ☒ a small entity.

2. Fee for Filing Brief on Appeal

Pursuant to 37 CFR 1.17(e), the fee for filing the Brief on Appeal is for: ☐ other than a small entity or ☒ a small entity.

Brief Fee Due $250.00

3. Oral Hearing

☐ Appellants request an oral hearing in accordance with 37 CFR 1.194.

CERTIFICATE OF MAILING

I hereby certify that this document (along with any documents referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Date: June 23, 2006

Christina Zemar

In re Appln. of Onody
Application No. 10/817,499

4. Extension of Time

☐ Appellants petition for a one-month extension of time under 37 CFR 1.136, the fee for which is $110.00

☒ Appellant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that appellant has inadvertently overlooked the need for a petition and fee for extension of time.

Extension fee due with this request: $

5. Total Fee Due

The total fee due is:

Brief on Appeal Fee	$250.00
Request for Oral Hearing	$ 0.00
Extension Fee (if any)	$ 0.00

Total Fee Due: $250.00

6. Fee Payment

☒ Attached is a check in the sum of $250.00.
☐ Charge Account No. 503594 the sum of $. A duplicate of this transmittal is attached.

7. Fee Deficiency

☒ If any additional fee is required in connection with this communication, charge Account No. 503594. A duplicate copy of this transmittal is attached.

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Date: June 23, 2006